Wrocław University of Technology, WPPT 26.03.07

AD HOC SYSTEMS, 2007 Problems, list # 2

1. Consider an MFSK scheme with $f_c = 250kHz$, $f_d = 25kHz$, and $M = 8$ ($L = 3bits$).
   (a) Make a frequency assignment for each of the eight possible data combinations.
   (b) We wish to apply FHSS to this MFSK scheme with $k = 2$. That is, the system will hop among four different carrier frequencies. Expand the results of part (1a) to show the $8X4 = 32$ frequency assignment.
2. Demonstrate that the codes in an 8x8 Walsh matrix are orthogonal to each other by showing that the product of any two codes is equal to 0.

   Consider a frame consisting of two characters of four bits each. Assume that the probability of bit error is 10^{-3} and that is independent for each bit.
   (a) What is the probability that the received frame contains at least one error?
   (b) Now add the parity bit to each character. What is the probability?
3. How many check bits are needed if the Hamming error correction code is used to tetect single bit error in a 1024-bit data word?
4. Divide $f(X) = X^6 + 1$ by $g(X) = X^4 + X^3 + X + 1$. Verify the result by multiplying the quotient by $g(X)$ to recover $f(X)$.
5. Using an interleaving structure of $n = 4$, $m = 6$, demonstrate each of the following block characteristics:
   (a) any burst of m contiguous channel bit errors results in isolated errors at the deinterleaver output that are separated from each other by at least m bits.
   (b) A periodic sequence of periodic sequence of single bit errors spaced m bits apart results in a single burst of errors of length n at the deinterleaver output.
   (c) Not including channel propagation delay, the interleaver end-to-end delay is $2(n(m-1)+1)$. Only $(n(m-1)+1)$ cells need to be filled before transmission can begin and a corresponding number needs to be filled at the receiver before deinterleaving can begin.
6. Consider a convolutional encoder defined by $v_{n1} = u_n + u_{n-2}$ and $v_{n2} = u_{n-1} + u_{n-2}$. Draw a shift register implementation for this encoder. Draw a state diagram for this encoder.
7. For the encoder in 6 assume that the shift register is initialized to all zeros and that after the transmission of the last information bit, two zero bits are transmitted. Why is that needed? What is the encoded sequence corresponding to the information sequence 1101011, read from left to right?

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